ABSTRACT OF THE DISCLOSURE

A method and system for generating a synchronous sequence of vectors from information originating within an asynchronous environment is disclosed. A simulated asynchronous sequence is synchronized by extracting a state at each clock period to generate a simulation synchronous sequence. This sequence is manipulated first to include short delays for generating an asynchronous short-delay sequence and second to include long delays for generating an asynchronous long-delay sequence. An overlay is separately performed among the clock periods of the asynchronous short-delay sequence and the asynchronous long-delay sequence to respectively identify a first interval and a second interval. The first interval and the second interval are independently duplicated in successive clock periods to respectively generate a synchronous short-delay sequence and a synchronous long-delay sequence. An overlay is performed on the two sequences to enable generation of the synchronous sequence of vectors for verifying operations of an IC design by a tester.